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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/083,447
Filing Date: February 26, 2002
Appellant(s): KISHIMOTO, KAZUNORI

Brian E. Hennessey
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/15/2006 appealing from the Office action mailed 4/29/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct except for new grounds outlined below.

New Grounds of Rejection

Whether or not claims 14-16 are unpatentable under 35 U.S.C. §101 as being written to non-statutory subject matter.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claims 1-4, 6-11 and 13-15 are rejected under 35 U.S.C. §103(a) as being unpatentable over the applicant's admitted prior art (herein AAPA), where references are taken from the originally presented Disclosure, "Background of the Invention", pages 1-13 (paragraphs [0001]-[0024]), and drawings FIG.5 through FIG.10 (subsequently

labeled as prior art), and in view of IEEE publication "Test Generation for Crosstalk-Induced Delay in Integrated Circuits" by Chen et al. (herein Chen).

Claims 5, 12, and 16-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over the applicant's admitted prior art, where references are taken from the Disclosure "Background of the Invention", pages 1-13 (paragraphs [0001]-[0024]), and drawings FIG.5 through FIG.10 (subsequently labeled as prior art), and in view of IEEE publication "Test Generation for Crosstalk-Induced Delay in Integrated Circuits" by Chen et al. (herein Chen), and further in view of Merrill, U.S. Patent No. 5235566.

Claims 1, 3-5, 7-12 and 14-16 are independent claims, and are the subject matter of interest in the appellant's arguments.

The independent claims in the application provide that the propagation delay time on a measurement path is measured by comparing or evaluating the actual value of a register at the end of the measurement path with an expected value. Such a feature is taught in the AAPA in FIG.6-10 and in the discussion of paragraphs [0004]-[0017] (the AAPA).

In particular, claim 1 relates to a method for testing a semiconductor integrated circuit (AAPA paragraph [0001]), when a signal for measuring a delay (for example, AAPA FIG.6 flip-flop 10_2 may be set to change the state of the input to flip-flop 10_5 through the combinational circuit as explained in paragraphs [0009] and [0010]), is applied to a measurement path (shown in FIG.6 flip-flop 10_5 begins the "measurement path") on which a delay test is conducted, a signal (for example, Chen, FIG.1 A_{in}, which would be an interfering signal within a comparable combinational circuit such as AAPA

FIG.6) having a transition being in phase (Chen FIG.1) or in opposite phase (Chen FIG.2) with the signal for measuring a delay (Chen FIG.1 V_{in}, which is comparable to the output of AAPA FIG.6 flip-flop 10_2) applied to the measurement path is applied to a path that influences crosstalk (Chen FIG.1 A_{in}) to the measurement path (see discussion in Chen page 193 section III). In this manner, a propagation delay time of the signal that propagates through the measurement path under the influence of crosstalk is measured (see AAPA paragraph [0020]). In the method according to claim 1, a propagation delay time of a signal is determined by comparing a value of a flip-flop (for example, AAPA flip-flop 10_8 in FIG.6) receiving the signal outputted from an output end of a measurement path (AAPA FIG.8 10_7 via measurement path 21, 22, 23) with an expected value (AAPA discussion paragraph [0020]).

Independent claim 3 relates to a method for testing a semiconductor integrated circuit in an AC test using a scan path. (AAPA, paragraph [0005]). The method includes receiving from a scan-in terminal of a scan path register (for example, AAPA FIG.8 SCAN IN) a pattern (Chen, page 192, column 1 paragraph 2) for supplying a signal for measuring a delay to a measurement path on which a delay test is conducted and a pattern for supplying a signal having a transition being in phase or in opposite phase with said signal for measuring a delay to a path that influences crosstalk to said measurement path (Chen, page 192 section II discussion on crosstalk). The method of claim 3 also includes supplying said signal for measuring a delay to said measurement path and supplying the signal to the path that influences crosstalk to said measurement path from said scan path register, and reading out a value of the scan path register that

samples said signal at an end terminal of said measurement path from a Scan-out terminal (in Chen, page 193 section III, PI's are set to cause delays to clock or data inputs of PO latches in the equivalent AAPA) to compare the value of said scan path register (the equivalent in AAPA is FIG.8 10_8) with an expected value, thereby measuring a delay time in said measurement path (for example, AAPA paragraph [0017]).

The present invention as recited in claim 4 relates to a method for testing a semiconductor integrated circuit having a scan path (see below), the measurement object being a clock signal (Merrill, column 1 lines 43-58, Abstract).

A method for testing a semiconductor integrated circuit having a scan path is recited in claim 5 (see below).

A method for testing a semiconductor integrated circuit having a scan path by a computer is recited in claim 7 (see below).

A method for generating patterns for testing a semiconductor integrated circuit having a scan path circuit by a computer is recited in claim 8 (see below).

An apparatus for generating patterns for testing a semiconductor integrated circuit having a scan path circuit is recited in claim 9 (see below).

An apparatus for generating patterns for testing a semiconductor integrated circuit having a scan path circuit is recited in claim 10 (see below).

A method for testing a semiconductor integrated circuit having a scan path circuit as a device under test with an LSI tester is recited in claim 11 (see below).

A method for testing a semiconductor integrated circuit having a scan path circuit as a device under test with an LSI tester as a testing device is recited in claim 12 (see below), the measurement object being a clock signal (Merrill, column 1 lines 43-58, Abstract)..

A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit is recited in claim 14 (see below).

A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit is recited in claim 15 (see below).

A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit is recited in claim 16 (see below), the measurement object being a clock signal (Merrill, column 1 lines 43-58, Abstract).

All of the independent claims 1, 3-5, 7-12 and 14-16 include a feature of "comparing a value of a flip-flop receiving said signal outputted from an output end of said measurement path with an expected value" (claims 1, 7, 8, 9, 10, 14), or similar feature, "comparing the value of said scan path register with an expected value, thereby measuring a delay time in said measurement path" (claim 3), "comparing a value of a flip-flop that samples the signal of an end terminal of said measurement path with an expected value, thereby measuring a delay time in said measurement path" (claims 4 and 5), "comparing the value of the flip-flop that receives the outputted signal outputted

fdrom the output end of said measurement path at the data terminal thereof with an expected value" (claims 11 and 12), and "comparing a value of a flip-flop receiving said signal propagated through said measurement path outputted from an output end of said measurement path with an expected value" (claims 15 and 16). These features are discussed in the AAPA, paragraphs [0001]-[0017] and FIG.6-10.

New Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

35 U.S.C. §101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 14-16 are rejected under 35 USC §101. The claimed invention in each of claims 14-16 is directed to non-statutory subject matter. The claims recite, "A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit, the program product comprising the processes of: ...". The limitations of each claim read to a list of activities per se being executed by a program, but the program as such is not embodied in a physical medium and therefore is not a physical "thing". The Federal Circuit recognizes that the fact that a nonstatutory method is carried out on a programmed computer does not make the process claim statutory. Grams, 888 F.2d at 841, 12 USPQ2d at 1829 (claim 16 ruled nonstatutory even though it was a computer-implemented process). Similarly, computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs, are not physical "things." They are neither computer

components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer which permit the computer program's functionality to be realized. In contrast, a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer program's functionality to be realized, and is thus statutory. See Lowry, 32 F.3d at 1583-84, 32 USPQ2d at 1035. Accordingly, the claims are rejected.

(10) Response to Argument

The applicant's arguments are rebutted herein as follows:

Whether or not claims 1-4, 6-11 and 13-15 are unpatentable under 35 USC §103(a) based on the AAPA in view of the Chen reference.

The appellant argued that there is no motivation to combine the subject references, but the examiner disagrees. The motivation is explicitly found in the reference Chen in page 191, column 2, where Chen states that severe design and test problems caused by crosstalk result in delays in product development and huge expenses. The advantage stated by Chen therein is a method to test for crosstalk that is a cost-effective alternative to expensive re-design of a chip during product development. The method, applied to standard circuit delay measurement methods, provides the manufacturer with a system that detects crosstalk (Chen page 193 section III). One with

ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to employ the crosstalk test method of Chen to the AAPA in order to speed product to the customer at lower cost.

The appellant further argued that neither Chen not the AAPA discloses comparing a flip-flop receiving a signal outputted from a measurement path under influence of crosstalk, but the examiner has shown above (see section 9 above, claim 1) that the AAPA and Chen, when combined, disclose the features.

Whether or not claims 5, 12 and 16-18 are unpatentable under 35 USC §103(a) based on the AAPA in view of the Chen reference, and further in view of Merrill.

The appellant argued that there is no motivation to combine the subject references, and that neither Chen not the AAPA discloses comparing a flip-flop receiving a signal outputted from a measurement path under influence of crosstalk. Both appellant arguments for these claims are the same as the arguments presented above in this section for claims 1-4, 6-11 and 13-15. These arguments are both answered by the examiner using the above answer in this section.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

This examiner's answer contains a new ground of rejection set forth in section **(9)** above. Accordingly, appellant must within **TWO MONTHS** from the date of this answer exercise one of the following two options to avoid *sua sponte* **dismissal of the appeal** as to the claims subject to the new ground of rejection:

(1) **Reopen prosecution.** Request that prosecution be reopened before the primary examiner by filing a reply under 37 CFR 1.111 with or without amendment, affidavit or other evidence. Any amendment, affidavit or other evidence must be relevant to the new grounds of rejection. A request that complies with 37 CFR 41.39(b)(1) will be entered and considered. Any request that prosecution be reopened will be treated as a request to withdraw the appeal.

(2) **Maintain appeal.** Request that the appeal be maintained by filing a reply brief as set forth in 37 CFR 41.41. Such a reply brief must address each new ground of rejection as set forth in 37 CFR 41.37(c)(1)(vii) and should be in compliance with the other requirements of 37 CFR 41.37(c). If a reply brief filed pursuant to 37 CFR 41.39(b)(2) is accompanied by any amendment, affidavit or other evidence, it shall be treated as a request that prosecution be reopened before the primary examiner under 37 CFR 41.39(b)(1).

Extensions of time under 37 CFR 1.136(a) are not applicable to the TWO MONTH time period set forth above. See 37 CFR 1.136(b) for extensions of time to reply for patent applications and 37 CFR 1.550(c) for extensions of time to reply for ex parte reexamination proceedings.

Respectfully submitted,

John P Trimmings

A Technology Center Director or designee must personally approve the new grounds of rejection set forth in section (9) above by signing below:

Jack B Harvey

Jack B. Harvey, Director
Technology Center 2100

Conferees:

Albert DeCady

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Emmanuel L Moise